Advanced Carrier Based Pulse Width Modulation in Asymmetric Cascaded Multilevel Inverter

Bambang Sujanarko  
Dept. of Elect. Eng., Universitas Jember, currently toward Doctor in Institut Teknologi Sepuluh Nopember (ITS) Surabaya, Indonesia

Mochamad Ashari  
Mauridhi Hery Purnomo  
Ontoseno Penangsang  
Soebagio  
Dept.of Elect. Eng., Institut Teknologi Sepuluh Nopember (ITS) Surabaya, Indonesia

Abstract – This paper proposes a new scheme Pulse Width Modulation (PWM) to overcome low performances of conventional PWM control strategy in Cascaded Multilevel Inverter (ACMLI). This scheme advance conventional Carrier-Based PWM (CBPWM) using triangle carrier in different amplitudes. By this scheme ACMLI can control by PWM that according to dc voltage amplitude used and finally the Total Harmonics Distortions (THD) can reduce to the settle standard. Simulation using Matlab Simulink used to verify the performance and result simulation shown than this proposed scheme can reach the goals.

Index Term-- asymmetric cascaded multilevel inverter, multi carrier pulse width modulation, power quality, total harmonic distortion.

I. INTRODUCTION

The multilevel inverter [MLI] is a promising inverter topology for high voltage and high power applications [1]. This inverter synthesizes several different levels of DC voltages to produce a staircase (stepped) that approaches the pure sine waveform [3-9]. Its have high power quality waveforms, lower voltage ratings of devices, lower harmonic distortion, lower switching frequency and losses, higher efficiency, reduction of dv/dt stresses and gives the possibility of working with low speed semiconductors if its comparison with the two-levels inverters. Numerous of MLI topologies and modulation techniques have been introduced and studied extensively, but most popular MLI topology is Diode Clamp, Flying Capacitor and Cascaded Multilevel Inverter (CMLI). In this paper we use a CMLI that consist of some H-Bridge inverters and with unequal DC. Its also namely Asymmetric Cascaded Multilevel Inverter (ACMLI). Its most implemented because this inverter more modular and simple construction and have other advantages than Diode clamp and flying capacitor [7].

There are many modulation techniques to control this inverter, such as Selected Harmonics Elimination or Optimized Harmonic Stepped-Waveform (OHSW), Space Vector PWM (SVPWM) and Carrier-Based PWM (CBPWM). Among these modulation CBPWM is the most used for multilevel inverter, because it have simple logical and easy to implemented. But if CBPWM used in the ACMLI, there is a problems, that is its have low power quality performance, so many method to adjust this controller find in many papers in the last decade.

To solve this problem, this paper propose a new scheme, which namely Advance Pulse Width Modulations (APWM). This scheme on behalf of PWM, but its not use triangle carrier waveform in equal amplitude as like to in the conventional PWM. The frequency and amplitude of triangle modulation must be according to amplitude of DC voltage on each H-Bridges inverter.

II. ACMLI

CMLI proposed to solve all the problems of the multilevel inverters as well as conventional multi pulse (or PWM) inverters [5-7]. CMLI eliminates the excessively large number of bulky transformers required by conventional multi pulse inverters, the clamping diodes required by multilevel diode clamped inverters, and the flying capacitors required by multilevel flying capacitor inverters.

CMLI consists a series connection of multiple H-bridge inverters. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter [3-4]. CMLI introduces the idea of using separate DC sources to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source. By cascading the output voltage of each H-bridge inverter, a stepped voltage waveform is produced [5-7]. If the number of H-bridges is N, the voltage output is obtained by summing the output voltage of bridges as shown in equation (1). Fig. 1 shows configuration of CMLI on single-phase.

Fig. 1. Single-phase cascaded multilevel inverter.
Using fig. 1, output voltage could express as (1). If ACMLI have N H-Bridges, there are many output voltages that produce from (1) with each H-Bridges has three varieties and has switching-states that appropriated on the voltages.

\[ V_o(t) = V_{o,1}(t) + V_{o,2}(t) + \ldots + V_{o,N}(t) \]  

In the CMLI, the DC voltage may or may not be equal to one another. If there are equal DC voltage, it namely symmetric CMLI and if there are un-equal DC voltage, it namely Asymmetric CMLI (ACMLI).

Binary and trinary DC voltages progressions are the most popular of unequal DC sources of ACMLI [4]. In binary progression and if the number of H-Bridge inverters are N, the amplitude of DC voltages having ratio 1: 2: 4: 8...: 2N and the maximum voltage output can equal (2N-1) Vdc. While in the trinary progression the amplitude of DC voltages having ratio 1: 3: 9: 27...: 3N and the maximum voltage output voltage reach to (3N-1)/2) Vdc. Other un-equal DC voltage is equal interval DC voltage progression. If \( N=2 \), the DC voltage are \( V_1=1, V_2=1/2 \); \( N=3 \), \( V_1=1, V_2=2/3, V_3=1/3 \); \( N=4 \), \( V_1=1, V_2=3/4, V_3=1/2, V_4=1/3 \); and \( N=5 \), \( V_1=1, V_2=4/5, V_2=3/5, V_3=2/5, V_5=1/5 \). ACMLI use sine quantization progression [2], also can used in the ACMLI where each DC voltage can be determined by equation (2). In this equation the voltage of sine wave reference is \( V_m \), the frequency is \( f \), the sequence

\[ V_{o,i} = V_m \sin(\omega t_i) \]

\[ = \frac{\sqrt{2}}{4N} \sin(2\pi f i) \]

\[ = \frac{\sqrt{2}}{2N} \sin(\frac{\pi f}{2N}) \]

\[ i = 1, 2, 3, \ldots, N \]  

IV. PROPOSES SCHEME AND DESIGN

The proposed scheme of advance CBPWM can show at Fig. 4. Each carrier wave in the CBPWM has amplitude of voltage peak to peak (vpp) that equal to each DC voltage. In this figure, vpp of carrier wave C3 equal to VDC3, vpp of C2 equal to VDC2, vpp of C1 equal to VDC1, and so also vpp in the negative phase.

Among other modulation, CBPWM strategies are the most popular methods used in CMLI, because they are easily implemented. Basic principle of CBPWM is sinusoidal pulse width modulation (SPWM), which uses a triangular carrier to generate the PWM as shown in Fig. 2.

CBPWM uses several triangle carrier signals, one carrier for each level and one reference, or modulation, signal per phase. CBPWM for three phases is shown in Fig. 3. In this figure shows the reference and carrier waveform arrangements necessary to achieve CBPWM for a seven levels inverter.

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Implementation this scheme in the circuit is similar to CBPWM conventional. The difference is only the amplitudes of triangle carrier. Fig. 5 shows block diagram of this circuit. This circuit then simulate with MATLAB/SIMULINK. Fig. 6 shows this circuit simulation. Among DC voltages progression, simulations done using
sine quantization DC voltage progression, because has optimum performance [3].

Amplitude of DC voltage in this simulation are $V_{dc5}=1$; $V_{dc4}=0.95$; $V_{dc3}=0.81$; $V_{dc2}=0.59$; $V_{dc1}=0.31$ (see eq. 2). While the amplitude of triangle are 3.66/5 for CBPWM in the conventional scheme and $V_{pp C5}=1$; $V_{pp C4}=0.95$; $V_{pp C3}=0.81$; $V_{dc2}=0.59$; $V_{dc1}=0.31$. Amplitude of sine reference in this simulation is 3.66V.

Each H-Bridges in ACMLI has power electronics as shown in Fig. 7. IGBT used in this circuit. In Fig. 8 shown detail of each CBPWM on each H-Bridges.

V. RESULT AND DISCUSSION

Results of simulations are shown in Fig.9 to Fig.12. Fig.9 is result simulation in the conventional CBPWM. In this system carrier triangle have equal amplitude, while the DC voltage have sine quantization as decrypted above. Its show that the waveform has fundamental amplitude 3.997 and THD in the frequency up to 1500 is 8.94%. The frequency spectrum this system is shown in Fig. 10.
Fig. 11 shows result of CBPWM was proposed in this paper. This result indicates that the proposed scheme can improve power quality, although this system only replaces the amplitudes of carrier triangle in the CBPWM conventional. Fundamental output voltage in this system has amplitude 3.663 and THD in the frequency up to 1500 Hz is 0.49%. While the spectrum frequency up to 1000 Hz in this system shows in Fig.12.

From Fig. 10 to Fig. 13, it show that the performance of the ACMLI more different, where the proposed scheme has better quality, especially to reduce THD. The different also happen in the other DC voltage progression.

CONCLUSION

A new scheme of CBPWM for ACMLI was proposed to improve the output voltage of CMLI. This scheme only replaces amplitude of carrier wave in the CBPWM according with amplitude of DC voltage that used in each H-Bridge. In the five H-Bridge of sine quantization ACMLI, THD can improve from 8.94 to 0.49%. Beside this power quality parameter, other parameter also can improve extremely, such as frequency spectrum and amplitude of fundamental output voltage.

REFERENCES


AUTHOR PROFILE

Bambang Sujanarko received the B.Sc. from Universitas Gadjah Mada, Yogyakarta Indonesia and Master from Universitas Jember, Indonesia. He is senior lecture of Departement Electrical Universitas Jember and currently toward his Ph.D in Institut Teknologi Sepuluh Nopember (ITS) Surabaya, Indonesia. His research interests included power electronics and renewable energy systems, hybrid power systems, artificial intelligent, and instrumentation.

Mochamad Ashari received the Bachelor degree in electrical engineering from the Institut Teknologi Sepuluh Nopember(ITS) Surabaya, Indonesia, in 1989 and Master and Ph.D. from Curtin University of Technology, Perth, Australia. He has been with ITS since 1990 as a Lecturer in the Department of Electrical Engineering. He is a Professor and head of Electrical Engineering ITS. His research interests include power electronics and inverter applications, power system modeling, simulation, and analysis of hybrid power systems.

Mauridhi Hery Purnomo received the B.S. degree from Institut Teknologi Sepuluh Nopember (ITS) Surabaya, Indonesia and Master ad Ph.D from Osaka City University, Osaka, Japan. He is a Professor in the Department of Electrical Engineering, ITS. Since 2007, he was vice director on ITS postgraduate program. He has been engaged in research and teaching in the areas of intelligent system and pattern recognition, power system simulations, and computer programming.

Ontoseno Penangsang is a Professor in the Department of Electrical Engineering, Institut Teknologi Sepuluh Nopember (ITS), Surabaya, Indonesia. He has been engaged in research and teaching in the areas of power system and electric power simulations.

Soebagyo is a Professor in the Department of Electrical Engineering, Institut Teknologi Sepuluh Nopember (ITS), Surabaya, Indonesia. He has been engaged in research and teaching in the areas of electric drive and electrical vehicles.