

CURRICULUM VITAE**MAHESH KUMAR SINGH**

Ho.No.-285,Sector-2C,Vasundhra
Ghaziabad(U.P.)

Email: mahesh.092002.ece@gmail.com

ramesh.sonu001@gmail.com

Phone No.09015584624,09793133257

CAREER OBJECTIVE

Pursuing a career where I can use my knowledge and skills to develop the applications which are useful to the academic and to the society.

EXPERIENCE

Working as Assistant Professor in Department of Electronics and Communication Engineering Babu Banarsi Das Institute of Technology, Ghaziabad (U.P.). from July 2011.

I have 1 Year 6 Months experience during my M.TECH. under Teaching assistantship in Jaypee University of Engg.& Technology GUNA (M.P.)

PROFESSIONAL SUMMARY

M. Tech: Electronics & Communication Engineering from (Jaypee University of Engg.& Technology GUNA (M.P.))

EDUCATION

| Education/Degree | University/Board | Percentage | Year |
|------------------|---|------------|------|
| M.Tech. | Jaypee University of Engg. & Technology Guna (M.P.) | 83.00 | 2011 |
| B.Tech. | U.P.T.U. Lucknow(U.P.) | 69.49 | 2009 |
| Intermediate | U.P. Board, Allahabad | 57.80 | 2003 |
| Highschool | U.P. Board, Allahabad | 59.67 | 2001 |

PROJECT**1-M.Tech.Thesis - Design & Implementation of Narrow Band Filter for ECG Signal**

Thesis Abstract-ECG signal processing is one of the hottest areas of research in Digital Signal Processing applications and Biomedical research. Analysis of ECG signals provides a crucial tool for diagnosis of heart diseases. The problem of ECG signal classification into healthy and pathological cases is primarily a pattern recognition problem using extracted features. Many methods of feature extraction have been applied to extract the relevant characteristics from a given ECG data. Design of Digital FIR filters design suitable for ECG application developed and implemented through VHDL in my dissertation.Design of FIR filter by Multirate Signal Processing using Decimator & Iinterpolator in this the complexity are less than the single stage FIR filter design. This implementation complexity are verified through VHDL.

TRAINING

1- Undergone Four weeks summer training in '*B.S.N.L Modinagar*,' in '**Telecommunication Department**.

2- Four Weeks Training In **Embedded Solutions**.

OTHERS ACTIVITY

Conferences

Attended Confer 2010-3rd CSI National Conference on Education & Research on "Impact of Globalization and Privatization on meeting India's IT Human Resource needs" Organized by Computer Society of India an IEEE MP subsection of Bombay Section.

SKILL SET/PROFILE

COMPUTER SKILLS:

Language : VHDL, MATLAB
Other tools : MS Word etc.

OTHER SKILLS:

- Willing to learn and apply my knowledge to practical situations.
- Good at planning, organizing events.

STRENGTHS

- Co-operative
- Self confident
- Flexible (can adjust to any circumstances)

HOBBIES

- Watching cricket
- Listening music

PERSONAL DETAIL

| | |
|----------------------|--------------------|
| Name | Mahesh Kumar Singh |
| Date of Birth | 06 December 1987 |
| Father's Name | Mr. Ram Singh |
| Nationality | Indian |
| Sex | Male |
| Marital status | Single |
| Language Proficiency | English, Hindi. |

DECLARATION

I, hereby declare that the above furnished particulars' are true to the best of my knowledge and belief if given chance, I will prove my efficiency, my loyalty & willingness to work in a good environment.

IJENS-RPG [IJENS Researchers Promotion Group]

Date:11/05/2012

Place:- Ghaziabad

ID: IJENS-1112-Mahesh

MAHESH KUMAR SINGH