FPGA-Based Global Positioning System

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***Abstract*— Global Positioning System (GPS) is a space based global navigation satellite system. It provides time and location information to users anywhere on earth. Nowadays, GPS is very useful for civil application and there is feasibility of enhancement for current tracking system. Hence, an offline tracking system is designed as the first phase of future online GPS. This paper presents the implementing of GPS on Field Programmable Gate Array (FPGA). The objective is to implement FPGA-based offline tracking system by parsing the GPS data using Verilog Hardware Description Language (Verilog HDL). The program is tested and simulated by using HDL compiler; Altera's Quartus® II Web Edition and Modelsim-Altera Starter Edition. The GPS data is then manipulated and implemented into FPGA board according to the required specification before they are finally filtered and manipulated to display on Liquid Crystal Display (LCD) module.**

***Index Term*— GPS, FPGA, Verilog HDL, tracking system**

I. INTRODUCTION

Global Positioning System (GPS) is a high-precision three-dimensional real time radio navigation system that used to determine accurate real time information. GPS system is widely used by land, sea and airborne users anywhere in the world and in all weather conditions. 24 hours working satellites are in orbit at 10,600 miles above the earth. They are spaced so that from any point on earth, four satellites will be above the horizon. Each satellite sends precise navigation messages to the ground continuously. The GPS receivers collect and process real time information to output accurate navigation data. Due to the advantages of global coverage, high precision and real-time positioning for all weather, GPS system is widely used in the search and rescue, traffic management, vehicle scheduling, land, sea and air navigation and positioning, survey and mapping all involved in the field of navigation positioning [1].

Verilog Hardware Description Language (Verilog HDL) is used in design, verification and implementation of digital system in a wide range of levels of abstraction. The language used to control the input and output of simulation [2]. It provides an alternative approach to design entry by letting the designer create a text description of the circuit without relying on a schematic. The language also defines constructs that can be used to control the input and output of simulation [6].

This paper introduces a real time GPS (Global Positioning System), offline tracking system based on FPGA. GPS signal is received continuously from GPS module. Altera DE2 Board is exploited as the host for the serial data packets from the GPS module. Verilog HDL is equipped with FPGA to manipulate raw data from GPS module. Data is extracted from GPS module and proceed to display on Liquid Crystal Display (LCD) of FPGA board.

II. SYSTEM AND MODULES INTRODUCTION

This section presents the system design and function modules that used in this FPGA-based GPS.

A. System Architecture

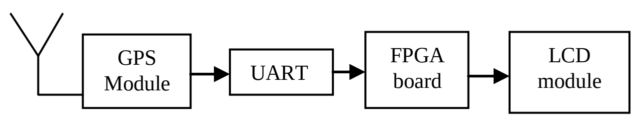

Fig. 1. System architecture.

Referring to Fig. 1, GPS signal is received by antenna and goes through GPS module by Universal Asynchronous Receiver/Transmitter (UART) using serial communication. UART receives the data and transmits them to Altera DE2 Board for further processes. Data packets received from GPS is filtered and selected. Not all the information from the GPS module is taken. Only the desired data sentence will be stored. All this process happened parallel with the process of checking the validation. The needed data is decoded in the physical layer and data packet is created in specific format before the data is transfer to Altera DE2 Board. The FPGA board continuously receives the data packets from GPS module and shows the contents of the data packets.

B. GPS Module

Holux GPSlim240 Wireless Bluetooth is a GPS receiver used in this project. It features two ways of communication with other systems; either via Bluetooth technology or USB serial communication using 38400 baud rate, 8 data bits, 1 stop bit and no parity bit [7]. The received signal from its antenna provides variety of information needed for any GPS data applications in the form of NMEA 0183 v2.2 protocol. This module is powered by the SiRF Star III chip.

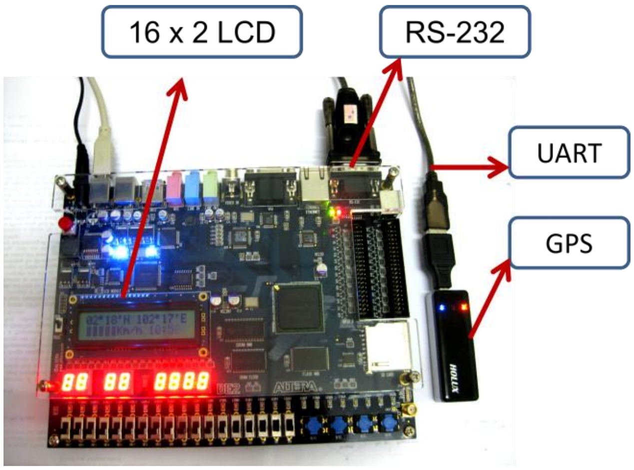

Fig. 2. Project overview.

C. Altera Development and Education 2 (DE2) FPGA Board

Altera DE2 Board (Fig. 2) is used to implement a wide range of designed circuits, from simple circuits to various multimedia projects. Software support for standard input and output (I/O) interfaces and a control panel facility for accessing various components are available for the board. For building this offline GPS, the board's features used in this project are:

- Altera Cyclone® II 2C35 FPGA device
- 16x2 LCD module
- RS-232 Port

D. Universal Asynchronous Receiver/Transmitter (UART)

Due to the different clock frequency of GPS module and the clock on Altera DE2 Board, UART is used as the connection bridge between them. UART receiver is taking the task of receiving the serial bit-stream of data, and transferring the individual bit of the byte in a sequential fashion [6]. The data arrives at a known standard bit rate but is not necessarily synchronized with the internal clock at the host of receiver, and the transmitter's clock is not available to the receiver. Thus, UART generates a local clock at a higher frequency and use it to sample the received data in a manner that preserves the integrity of the data [9].

E. Liquid Crystal Display Module

Liquid Crystal Display (LCD) module is an electronic flat panel display. Altera DE2 Board's LCD module has built-in fonts and can be used to display text by sending appropriate commands to the display controller [10]. The LCD module will then shows the information extracted from serial data packets received previously in the NMEA 0183 v2.2 protocol.

F. GPS Output Format

Holux GPSlim240 Wireless Bluetooth communication is defined within NMEA-0183 v2.2 specification. There are two types of data generated for every one second and every five seconds commonly called as sentences. Each sentence starts with a dollar sign character. The next five characters identify the talker (two characters, GP) and the format of sentence (three characters). The output formats are in GGA, RMC, GSA, GSV and VTG. GGA, RMC and VTG are generated one a second, whereas GSA and GSV produced by the GPS once for every five seconds. All data fields that follow are comma-delimiter. The Null bytes will be occurring when data is unavailable. The maximum characters allowed are 82 characters in one sentence [7]. The end of a sentence is marked by the asterisk character and followed by a two-digit hexadecimal checksum number for that particular sentence before end of line <CR><LF> characters. In this project, header GGA, RMC and VTG are used to extract the desired data.

III. Implementation and Software

Two main software used to design the project are Altera's Quartus® II Web Edition and Modelsim-Altera Starter Edition. The real time offline GPS system was implemented on the Altera DE2 Board.

A. System Program Flow (Fig. 3)

The system starts with the initialization of the UART module (38400 baud rate, 8 data bits, 1 stop bit and no parity bit). The data received at the end of the end of communication line are in Bytes form.

When data byte is received, the flow proceeds for filtering the data header. Five types of data header from GPS module are GGA, GSA, GSV, RMC, and VTG. Every GPS sentence starts with a '$' sign character and end with end of line <CR><LF>. Only three types of data sentences are needed to be filtered and to be used in this project; GGA, RMC and VTG. Thus, headers that are filtered and used will be '$GPGGA', '$GPRMC', and '$GPVTG'.

Altera DE2 Board continuously receives the data packets from GPS Module and shows the contents of the GPS sentences. In each sentence, the checksum is the resultant of exclusive-OR of all characters between the '$' character and '*' character. The resultant is then compared to the last two ASCII characters of sentence before end of line <CR><LF>. The process of filtering the sentences header and comparing the checksum are done simultaneously.

Next, each sentence is decoded in the physical layer. There are 14 valuable data items stored in GGA sentence. The 2nd (latitude value), 3rd (latitude indicator/unit), 4th (longitude value) and 5th items (longitude indicator/unit) in GGA sentence are extracted. For RMC sentences, the 1st (time in 24-hours format) and 9th item (date) are decoded and finally the data extracted from VTG sentence are the 7th items which contain the speed value.

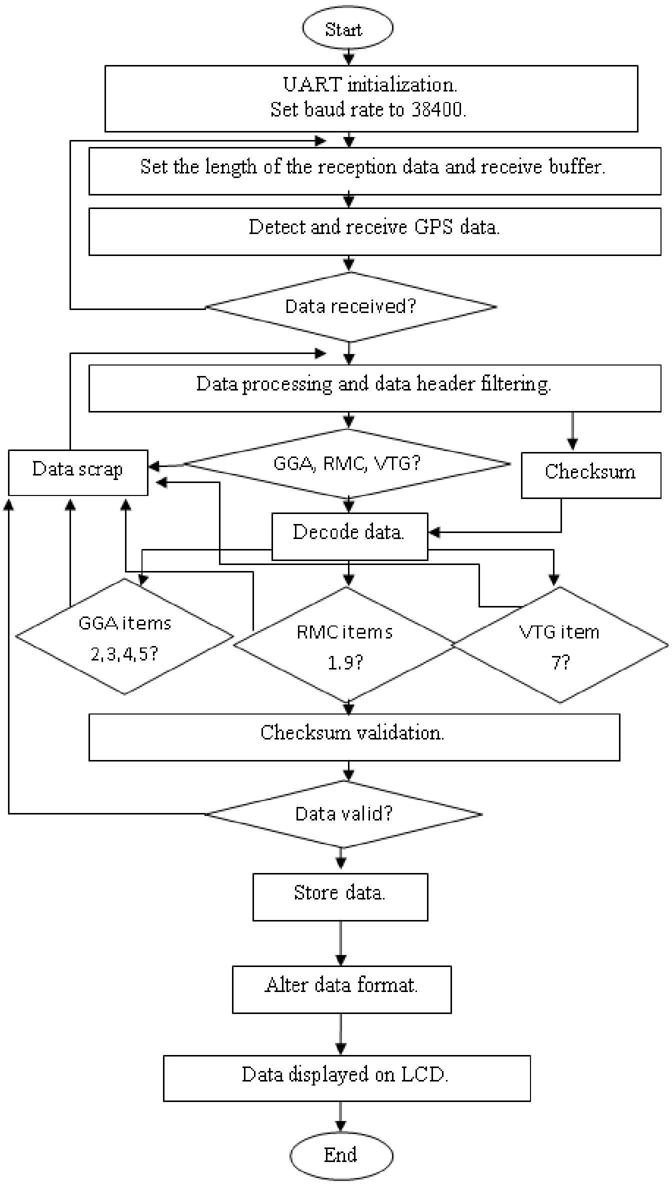

Fig. 3. Flow chart of project program.

Data items with checksum error are neglected. Only the valid data items are filtered and to be processed to display on the LCD module.

B. Data Decoding

GPS sentences received from GPS Module through UART, will be extracted from serial data packets. For example, real time GPS receiver will extract the $GPGGA sentence:

$GPGGA,211701.307,3610.5124,N,08530.4004,W,1,05,7.4,390.3,M,-30.9,M,,*6E

The extracted data items (latitude and longitude) from the sentence above are "3610N" as the latitude information and "08530W" as the longitude information. "3610N" presents the latitude as 36 degree and 10 minutes of North. Likewise, "08530W" presents the longitude as 85 degree and 30 minutes of West.

B. Program Debugging

Completed design program is compiled to check the synthesizable of the coding. The design system and program is downloaded into Altera Cyclone II EP2C35F672 FPGA chip. The target device is important to be checked before downloading operation to make sure correct version of FPGA is used. The execution for the program into FPGA must be made sure without errors. Warnings are allowed but there are risks of unnecessary problem in prototype functionality. After finishing the whole synthesizing process without any error, the device was booted by using Programmer in Altera's Quartus® II Web Edition [11]. A '.SOF' file will be generated after all compilation are done. After program succeeded, the output of the GPS data could be observed from the LCD Module on the board.

IV. Results

Extracted and decoded data items from GPS sentences are latitude, longitude, speed and time. The detected information is displayed on the 16 x 2 LCD on Altera DE2 Board. The first row of LCD displayed: latitude and latitude indicator, longitude and longitude indicator. Speed and time were displayed on second row of LCD screen.

V. Conclusion

This paper presents the implementation offline GPS based on GPS module and Altera DE2 FPGA board. This project can effectively extract the information from all the GPS data and saving resources. By using Verilog HDL on FPGA, simply write a few of behavioral model and simulate it with test benches, synthesize it and finally downloads it into FPGA [8]. It is very convenient as this GPS could be easily upgraded to better functionality by using FPGA [5]. Thus, FPGA-based GPS is a good choice as it is easy to be designed and upgradable in future. Compared to the conventional orientation navigation system, the advantages are: using the FPGA which leads to high integration, low power consumption, low cost, short development cycle, convenient to upgrade the product and long life cycle [3][4]. It has great future in fields such as car navigation, transportation, fieldwork, public security, electric power, and the metallurgy industry.

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