

# Closed-Loop Derivation and Evaluation of Joint Carrier Synchronization and Channel Equalization Algorithm for OFDM Systems

Chih-Feng Wu and Muh-Tian Shiue

**Abstract**— This paper emphasizes how to establish the signal flow graph (SFG) of joint carrier synchronization and channel equalization algorithm for OFDM baseband inner receiver using the *multirate* digital phase-locked loop (DPLL) and the *fictitious sampler* techniques. Therefore, the closed-loop transfer function (TF) can be easily derived and further applied to examine the stability and the performance of OFDM baseband receiver.

**Index Term**— Orthogonal frequency division multiplexing (OFDM), carrier frequency offset (CFO), digital phase-locked loop (DPLL)

## I. INTRODUCTION

The joint carrier synchronization and channel equalization algorithm [1]-[2] was presented to simultaneously combat the residual carrier frequency offset (CFO) and the channel distortion for orthogonal frequency division multiplexing (OFDM) systems in the *tracking stage* over the multipath frequency-selective fading channel. Theoretically, the joint algorithm is constructed of a carrier synchronization and a gain equalization schemes. The block diagram of joint algorithm is illustrated in Fig. 1. Furthermore, the carrier synchronization scheme is a *dual-loop* structure, which is composed of *inner* and *outer* loops, with *multirate* processing. Both *inner* and *outer* loops can be viewed as *frequency*- and *phase*-tracking loops, respectively.

In order to evaluate the stability and the performance of the presented carrier synchronization and gain equalization loops, the *Nichols* chart and the *jitter* analysis are examined in [1]-[2] based on the transfer function (TF). Therefore, the formation of signal flow graph (SFG) is crucial to derive the closed-loop, the open-loop and the noise TFs. Furthermore, the *Nichols* chart can be obtained according to the *open-loop* TF. The *jitter* analysis can be acquired from the *closed-loop* and the *noise* TFs.

In this paper, the formation of signal flow graph (SFG) of joint algorithm for OFDM baseband inner receiver is presented

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based on the *multirate* digital phase-locked loop (DPLL) and the *fictitious sampler* techniques. Consequently, the closed-loop transfer function (TFs) of multirate carrier synchronization and gain equalization loops can be easily derived and further applied to evaluate the stability and the performance of OFDM baseband receiver as presented in [1]-[2]. The paper is organized as follows: The signal model of the proposed joint algorithm is briefly introduced in section II. The establishment of SFG for the joint algorithm are described and the TFs are derived in section III. Then, the simulation results are shown in section IV. Finally, the conclusions are given in section V.

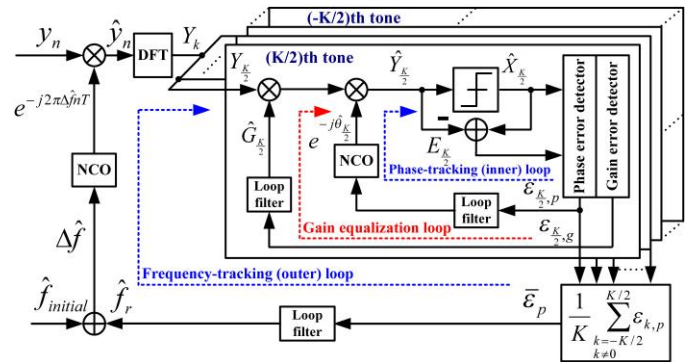


Fig. 1. Block diagram of joint carrier synchronization and channel equalization algorithm for OFDM baseband inner receiver.

## II. JOINT CARRIER SYNCHRONIZATION AND CHANNEL EQUALIZATION ALGORITHM

### A. MMSE Criterion and Cost Function

The minimization of mean square error (MSE) on each subchannel is crucial to increase the system performance for OFDM systems. Based on the minimum MSE (MMSE) criterion, the joint algorithm is presented to minimize the MSE on each subchannel. Thus, the cost function  $J(\cdot)$  [2] is given by

$$\arg \min_{\hat{G}_k, \hat{\theta}_k} J(\hat{G}_k, \hat{\theta}_k) = \mathcal{E}_k = \mathbf{E}[|E_k|^2] \quad (1)$$

where  $\mathbf{E}[\cdot]$  is an expectation operator.  $\mathcal{E}_k$  and  $E_k$  denote the MSE and the decision error on the  $k$ th subchannel, respectively. Furthermore,  $E_k = X_k - \hat{Y}_k$ , where  $X_k$  and  $\hat{Y}_k$  are the desired and the equalized signals on the  $k$ th subchannel.

Significantly, both  $\widehat{\mathbf{G}}_k$  and  $\widehat{\boldsymbol{\theta}}_k$  are employed to compensate the magnitude  $\mathbf{G}_k$  and the phase  $\boldsymbol{\theta}_k$  distortions caused by the CFO  $\Delta\mathbf{f}$  and the channel impairment  $\mathbf{H}_k$  on the  $k$ th subchannel. Eq. (1) indicates that the precise gain and phase can minimize the error power  $\boldsymbol{\varepsilon}_k$  to achieve the maximum subchannel SNR, i.e.,  $\text{SNR}_k = \mathbf{S}_k/\boldsymbol{\varepsilon}_k$  where  $\mathbf{S}_k$  is the signal power of  $k$ th subchannel. Consequently, the closed-loop control technique [5] is employed to realize the joint algorithm to acquire the exact gain and phase.

### B. Signal Model

The characteristics of joint algorithm are briefly introduced in the following,

- **Outer Loop:** The loop is employed to obtain  $\widehat{\mathbf{f}}_r$  to remove the linear increment of phase offset for the  $n$ th received sample  $\mathbf{y}_{n,l}$  at the  $l$ th OFDM symbol in the time domain. Therefore, a *frequency subtractor* is performed by a *derotator* to acquire CFO error  $\mathbf{f}_e = \Delta\mathbf{f} - \widehat{\Delta\mathbf{f}}$ , where  $\widehat{\Delta\mathbf{f}}$  is the estimated CFO. The *derotator* output can be represented as

$$\widehat{\mathbf{y}}_{n,l} = e^{-j\widehat{\phi}_n} \cdot \underbrace{[\mathbf{y}(t) \cdot e^{-j2\pi\Delta\mathbf{f}t}]_{t=l(N+N_g)T+N_gT+nT}}_{\mathbf{y}_{n,l}} \quad (2)$$

where  $\widehat{\phi}_n = 2\pi\Delta\widehat{\mathbf{f}}nT$ .  $\Delta\widehat{\mathbf{f}} = \Delta\widehat{\mathbf{f}}_{\text{initial}} + \Delta\widehat{\mathbf{f}}_r$ , where  $\Delta\widehat{\mathbf{f}}_{\text{initial}}$  is obtained in the *initial acquisition* stage including the *coarse* and the *fine* CFO estimations. The  $\mathbf{y}(t)$  is the channel output signal with continuous time. Both  $N$  and  $N_g$  are the number of point of DFT and the sample length of guard interval, respectively. Besides,  $T$  is a sample interval and equal to  $T_u/N$ , where  $T_u$  is a DFT duration. After the derotator operation, the  $\mathbf{f}_e$  is further transferred by DFT to be the normalized CFO error  $\boldsymbol{\varepsilon}_e = \mathbf{f}_eNT$ , which results in the constellation rotation on each subchannel, in the frequency domain.

- **Inner Loop:** After completing the DFT operation, the  $k$ th subchannel of the  $l$ th received symbol can be reformulated as

$$\mathbf{Y}_{k,l} \approx \mathbf{G}_{k,l} \cdot e^{-j\boldsymbol{\theta}_{k,l}} \cdot \mathbf{X}_{k,l} + \mathbf{V}_{k,l} \quad (3)$$

where  $\mathbf{X}_{k,l}$  and  $\mathbf{V}_{k,l}$  are the transmitted symbol and the additive white noise, respectively, on the  $k$ th subchannel. The inner loop is used to eliminate the constellation rotation caused by  $\boldsymbol{\theta}_{k,l}$  on the  $k$ th subcarrier in the frequency domain. Actually,  $\boldsymbol{\theta}_{k,l}$  is composed of  $\boldsymbol{\varepsilon}_e$  and  $\boldsymbol{\theta}_{\mathbf{H}_{k,l}}$ , where  $\boldsymbol{\theta}_{\mathbf{H}_{k,l}}$  is the phase distortion of multipath fading channel on the  $k$ th subchannel.

- **Gain Equalization Loop and Subchannel Output:** The gain equalization loop is employed to remove the magnitude distortion  $\mathbf{G}_{k,l}$  of multipath fading channel

on the  $k$ th subchannel. Finally, the reparation output on the  $k$ th subchannel can be expressed

$$\widehat{\mathbf{Y}}_{k,l} = \widehat{\mathbf{G}}_{k,l} \cdot e^{-j\widehat{\boldsymbol{\theta}}_{k,l}} \cdot \mathbf{Y}_{k,l} \quad (4)$$

where  $\widehat{\mathbf{G}}_{k,l}$  and  $\widehat{\boldsymbol{\theta}}_{k,l}$  are used to resist the magnitude and the phase distortions, respectively.

## III. SIGNAL FLOW GRAPH AND TRANSFER FUNCTION

### A. Multirate Carrier Synchronization Loop

In order to establish SFG, the enlightened viewpoints for the multirate carrier synchronization loop are described as follows:

- **Digital Mixers and Subband Filters:** DFT can be regarded as a combination of  $N$  digital mixers and  $N$  unit gain subband filters. The related phase and gain of the subband filter are merged into the subchannel response  $\mathbf{H}_{k,l}$  in *polar coordinate* such as  $\boldsymbol{\theta}_{\mathbf{H}_{k,l}}$  and  $\mathbf{G}_{\mathbf{H}_{k,l}}$ , respectively. Considering a complete OFDM symbol with  $N_s$  samples, the DFT operation only processes  $N$  data samples since  $N_g$  samples were discarded previously. Moreover, the bandwidth (BW) of the multirate carrier synchronization loop is much less than that of the subband filter. Therefore, DFT can be reasonably ignored and modeled by a down-sampling with ratio  $N_s:1$ .
- **Inner Loop:** The loop is constructed on each subcarrier to fulfill Eq. (4). Actually, the inner loop is operated in the symbol-rate  $1/T_s$  region. The feedback loop from the inner loop to the outer loop has to be up-sampled from the symbol-rate to the sample-rate. Therefore, the up-sampling operation is accomplished by a *hold process* [5] with ratio  $1:N_s$ .
- **Outer Loop:** The loop strides across the sample-rate and the symbol-rate regions. Practically, the outer loop performs Eq. (2) at the sample-rate  $N_s/T_s$  region in the time domain. Subsequently, the phase error of Eq. (2) will be transferred to the frequency domain and down-sampled to the symbol-rate region. There are  $K$  inner loops operating at the symbol-rate region within the outer loop. Without loss of generality, the  $K$  inner loops can be simplified to a single loop  $\mathbf{H}_{in}(z)$  since the phase error resulted from CFO is independent of the subcarrier index.
- **Phase Error Detector (PED):** The error detector performs the cross-correlation between the desired signal and the decision error to extract the phase error information on each subcarrier. Therefore, the PED can be expressed as  $\boldsymbol{\varepsilon}_{k,p} = \mathfrak{I}\{\widehat{\mathbf{X}}_k \mathbf{E}_k^*\}$  with gain  $\boldsymbol{\kappa}_d$  where  $*$  is a complex conjugate operation. Apparently, the PED is also operated in the symbol-rate region.

As mentioned above, the SFG of the multirate carrier

synchronization loop can be illustrated in Fig. 2. Two different variables of  $z$ -transform are used to represent the multirate processing:  $z$  in the symbol-rate region and  $\eta = z^{1/N_s}$  in the sample-rate region. Both  $\kappa_o$  and  $\kappa'_o$  express the numerically controlled oscillator (NCO) gains of the outer and the inner loops, respectively.  $\kappa_i$  and  $\kappa_p$  denote the gains of integral- and proportional-controller, respectively. In addition, the noise source  $V(z)$  as shown in Fig. 2 is considered for the presence of noise in the closed-loop. All elements in Fig. 2 are assumed quasilinear process [5] to derive  $z$ -domain TFs. The open loop model with two transform variables of the multirate carrier synchronization loop is shown in Fig. 3.

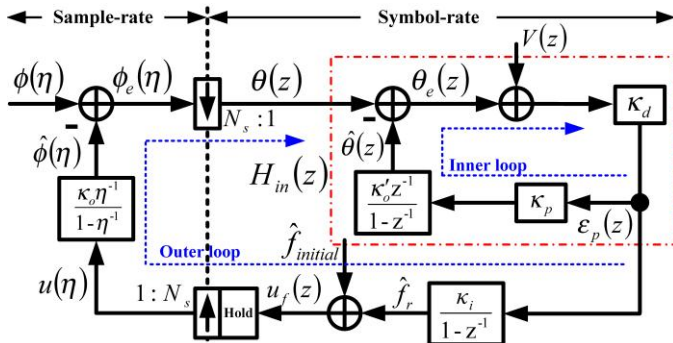


Fig. 2. Signal flow graph of multirate carrier synchronization loop.

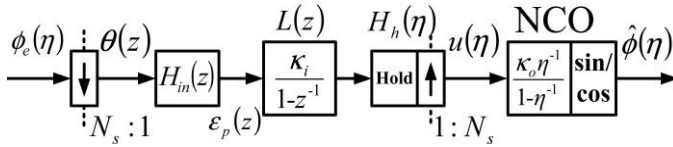


Fig. 3. Open loop model of multirate carrier synchronization loop with two transform variables.

**1) Fictitious Sampler Technique:** In order to handily derive TFs, the multirate processing scheme in SFG has to be transferred to a fixed-rate processing. Consequently, the elements operating in the sample-rate region have to be converted to the symbol-rate region using *fictitious sampler* method [5]. It is worth noting that the *fictitious sampler* is only for analytical assumption and expedient.

A *fictitious up-sampler* with ratio  $1:N_s$  is inserted in the preceding of the phase subtractor as depicted in Fig. 4. From the *fictitious up-sampler* point of view, the input sequences  $\dots, \phi_m, \phi_{m+1}, \dots$  become  $\dots, \phi_m, \phi_{m+1/N_s}, \dots, \phi_{m+(N_s-1)/N_s}, \phi_{m+1}, \dots$ . This model indicates that  $\phi_m$  is unchanged in  $\phi_{m+i/N_s}$  for  $i = 0 \sim (N_s - 1)$ . Similarly, a *fictitious down-sampler* with ratio  $N_s:1$  is also inserted in the succeeding of the phase subtractor as depicted in Fig. 4. Practically, the current  $\Delta\hat{f}$  as shown in Fig. 1 is acquired at the symbol-rate  $1/T_s$ , namely, the *hold process* keeps the current  $\Delta\hat{f}$  for a symbol interval  $T_s$ . Therefore,  $\phi_e$  also retains for a symbol interval since the relationship between  $\phi$  and  $\hat{\phi}$  is not changed from sample to sample for a symbol interval.

Based on the *fictitious sampler* method, the open loop model with two transform variables as shown in Fig. 3 can be converted to a single transform variable as shown in Fig. 5. Significantly,  $\theta(z)$  is equivalent to  $\alpha\phi_e(z)$  according to the *fictitious sampler* as described in Fig. 4. In addition,  $\alpha$  is a scaling factor, which expresses the gain scaling induced by DFT. Physically,  $\alpha$  is assumed to be  $1$  and further the related gain scaling is lumped into the loop gain.

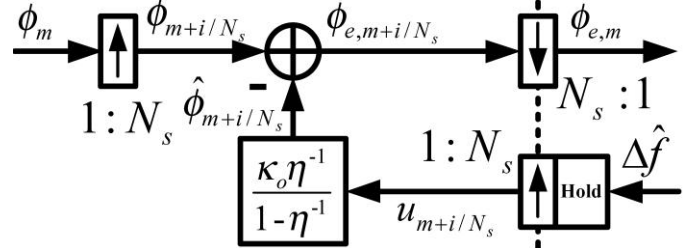


Fig. 4. Model for a fictitious up-sampler and down-sampler.

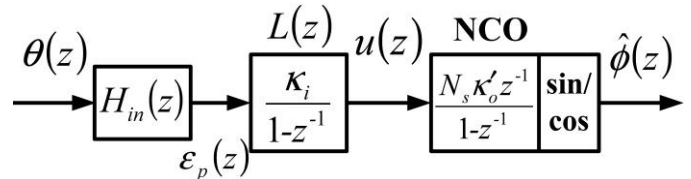


Fig. 5. Open loop model of multirate carrier synchronization loop with a single transform variable.

**2) Transfer Function Derivation:** Without loss of correctness,  $V(z)$  as depicted in Fig. 2 is assumed zero to derive TFs. Therefore, the related TFs of the multirate carrier synchronization loop can be acquired based on the SFG and the open-loop model as shown in Fig. 5.

- **Inner Loop:** The loop is employed to extract  $\hat{\theta}_k$  to immediately minimize the phase error  $\theta_{e,k} = \theta_k - \hat{\theta}_k$ . Therefore, the loop filter is realized using a *proportional* controller with gain  $\kappa_p$ . As a result, a **type-1 DPLL** is used to construct the inner loop. The phase and the phase error TFs can be derived as

$$H_i(z) = \frac{\hat{\theta}(z)}{\theta(z)} = \frac{\kappa_1}{z - (1 - \kappa_1)} \quad (5)$$

$$E_i(z) = \frac{\theta_e(z)}{\theta(z)} = \frac{z - 1}{z - (1 - \kappa_1)} \quad (6)$$

where  $\kappa_1$  is an open loop gain and equivalent to  $\kappa_d \kappa'_o \kappa_p$ . The subscript  $k$  is ignored in Eq. (5) and (6) since all subchannels have the same  $\kappa_1$ . On the other hand, the inner loop TF  $H_{in}(z)$ , which is depicted with dash-dot line as shown in Fig. 2, can be expressed as

$$H_{in}(z) = \frac{\varepsilon_p(z)}{\theta(z)} = \kappa_d E_i(z) = \frac{\kappa_d(z - 1)}{z - (1 - \kappa_1)} \quad (7)$$

- **Outer Loop:** From the carrier frequency synchronization point of view, the loop is employed to acquire  $\hat{f}_r$  to minimize the carrier frequency error  $f_e$ . Therefore, the loop filter is realized by an *integral* controller with gain  $\kappa_i$ . A **type-2 DPLL** is used to carry out this task.

Before derivation of outer loop TF, the open loop TF  $F(z)$  with the single transform variable as shown in Fig. 5 is derived as

$$F(z) = \frac{\hat{\phi}(z)}{\phi_e(z)} = \frac{\kappa_2 z}{(z-1)[z-(1-\kappa_1)]} \quad (8)$$

where  $\kappa_2 = \kappa_d \kappa_o \kappa_i$ . According to Eq. (8), the phase and the phase error TFs of outer loop can be expressed as

$$H_o(z) = \frac{\hat{\phi}(z)}{\phi(z)} = \frac{F(z)}{1+F(z)} \quad (9)$$

$$= \frac{\kappa_2 z}{(z-1)[z-(1-\kappa_1)] + \kappa_2 z}$$

$$E_o(z) = \frac{\phi_e(z)}{\phi(z)} = \frac{1}{1+F(z)} \quad (10)$$

$$= \frac{(z-1)[z-(1-\kappa_1)]}{(z-1)[z-(1-\kappa_1)] + \kappa_2 z}$$

- **Dual Loop:** The multirate carrier synchronization scheme can be viewed as a *dual-loop* structure since the synchronization scheme not only tracks the residual CFO within the outer loop in the time domain but also recovers the normalized residual CFO and the channel phase variation within the inner loop in the frequency domain. Therefore, the phase and the phase error TFs of *dual-loop* can be derived as

$$H_d(z) = \frac{\hat{\theta}(z)}{\phi(z)} = \frac{\hat{\theta}(z)}{\phi(z)} \cdot \frac{\phi_e(z)}{\phi(z)} \quad (11)$$

$$= \frac{\kappa_1(z-1)}{(z-1)[z-(1-\kappa_1)] + \kappa_2 z}$$

$$E_d(z) = \frac{\theta_e(z)}{\phi(z)} = \frac{\theta_e(z)}{\theta(z)} \cdot \frac{\phi_e(z)}{\phi(z)} \quad (12)$$

$$= \frac{(z-1)^2}{(z-1)[z-(1-\kappa_1)] + \kappa_2 z}$$

Obviously, Eq. (11) indicates that the TF of dual-loop is identical with that of traditional type-2 DPLL [5]. The inner- and outer-loop of dual-loop structure can be regarded as *proportional*- and *integral*-part of DPLL, respectively. In consequence, the *proportional*-controller, constructed on each subcarrier, can instantly respond and compensate to the variation of phase distortion  $\theta_{k,l}$ . The *integral*-controller, built on the outer-loop, is employed to track the residual CFO and further minimize the CFO error  $f_e$ .

### B. Gain Equalization Loop

The first-order gain equalization loop is constructed on each subchannel to compensate the magnitude distortion. The SFG of gain equalization loop is illustrated in Fig. 6, where  $V(z)$  is noise source. The gain error detector (GED) is acquired by  $\varepsilon_{k,g} = \Re\{\hat{\mathbf{X}}_k \mathbf{E}_k^*\}$ , which reflects the signal power difference between the decision data  $\hat{\mathbf{X}}_k$  and the equalized signal  $\hat{\mathbf{Y}}_k$ . Therefore, the gain equalization loop on each subchannel can be expressed as

$$\hat{\mathbf{G}}_k(l) = \hat{\mathbf{G}}_k(l-1) + \mu_g \cdot \varepsilon_{k,g}(l-1) \quad (13)$$

where  $\mu_g$  is an open loop gain step-size. The closed-loop TF can be derived as

$$H_g(z) = \frac{\mu_g}{z-(1-\mu_g)} \quad (14)$$

The subscript  $k$  is dropped in Eq. (14) since  $\mu_g$  is the same for all subchannels.

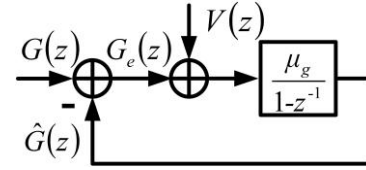


Fig. 6. Signal flow graph of gain equalization loop.

### C. Noise Transfer Function

In view of the performance degradation induced from the phase  $\Delta\theta$  and the gain  $\Delta G$  errors in the steady-state tracking stage over the frequency-selective fading channel, the closed-loop jitters of multirate carrier synchronization and gain equalization loops should be evaluated by the averaged SNR [2]. Consequently, giving a noise source at  $V(z)$  and assuming zero input at  $\phi(z)$  and  $G(z)$ , the noise TFs of both loops can be described as

$$H_{n,d}(z) = \frac{\theta_e(z)}{V(z)} = \frac{-\kappa_2 z - \kappa_1(z-1)}{(z-1)[z-(1-\kappa_1)] + \kappa_2 z} \quad (15)$$

$$H_{n,g}(z) = \frac{G_e(z)}{V(z)} = \frac{-\mu_g}{z-(1-\mu_g)} \quad (16)$$

### D. Summary

Based on Eq. (11) and (14), the closed-loop approximations for multirate carrier synchronization and gain equalization loops can be easily derived. Therefore, the closed-loop parameters including  $\kappa_1$ ,  $\kappa_2$  and  $\mu_g$  can be handily obtained. In order to examine the system stability of dual-loop, the Nichols chart is employed to evaluate the phase and the gain margins by using the open-loop TF  $F(z)$ . Besides, the closed-loop jitters of both loops can be acquired according to the noise TFs as shown in Eq. (15) and (16). The detail descriptions for the closed-loop approximation, the system stability and the closed-loop jitter can be found in [12].



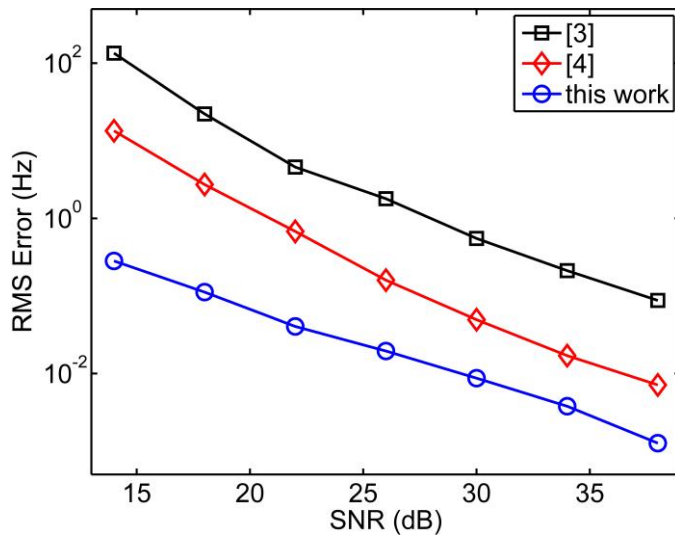
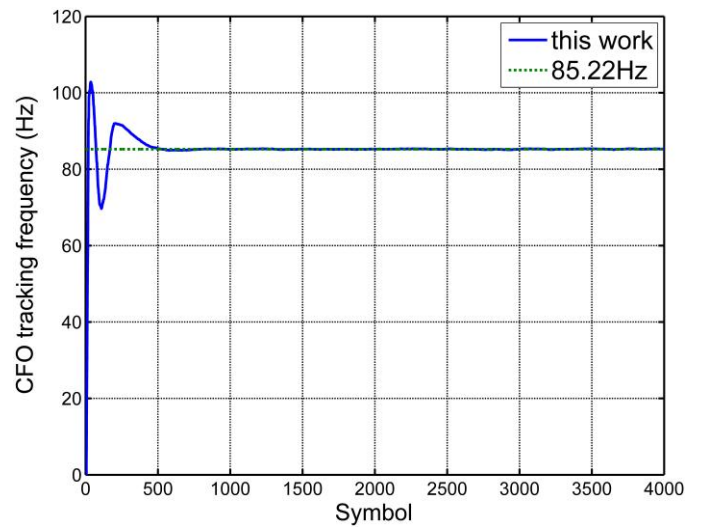


Fig. 7. CFO RMS errors vs. different SNR levels with CFO=-232.2 KHz.

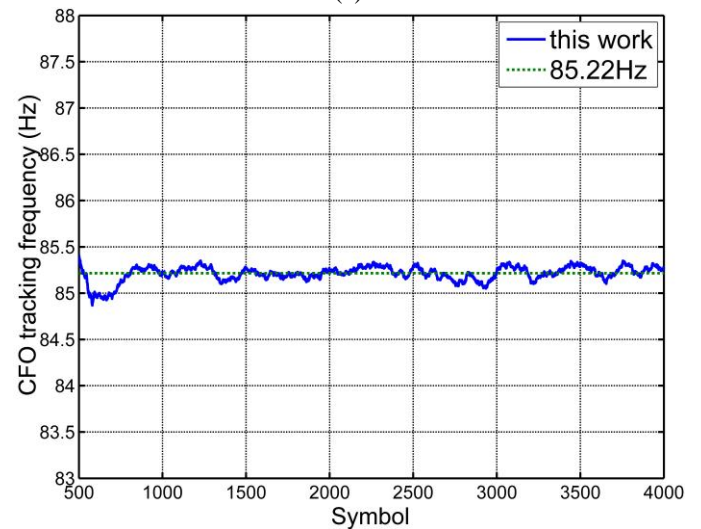
#### IV. SYSTEM SIMULATION

A test vehicle, OFDM transceiver for IEEE 802.11a WLAN, is used to demonstrate the reliability of the joint carrier synchronization and channel equalization algorithm. The multipath fading channel is derived from [6] with the median delay spread 50 ns in office building. In order to demonstrate the tracking capability in the different SNR levels for the joint algorithm, CFO root-mean-square (RMS) error is adopted as a performance indicator as illustrated in Fig. 7. The improvements of CFO RMS error for the joint algorithm to the previous works ([3] and [4]) are about 40 dB and 20 dB, respectively.

The trajectory of CFO tracking is shown in Fig. 8. The residual CFO remains 85.22 Hz after the coarse and fine CFO acquisitions in the short- and long-preamble respectively. The overshoot as shown in Fig. 8 (a) in the initial tracking does not affect the data decision since the effect can be immediately recovered by the inner loop on each subchannel. The enlarged plot in the steady-state from 500th to 4000th symbol is also illustrated in Fig. 8 (b) to exhibit the frequency error is less than  $\pm 1$  Hz.



(a)



(b)

Fig. 8. Trajectory of CFO tracking in multipath fading channel with CFO=-232.5 KHz. (a) tracking from initial tracking to steady state and (b) tracking in the steady state.

#### V. CONVLUSION

The closed-loop derivation of the joint carrier synchronization and equalization algorithm for OFDM systems in the *tracking stages* is presented using the *multirate DPLL* and the *fictitious sampler* techniques. The derivation of multirate carrier synchronization loop includes the formation of SFG, the transformation of  $z$ -domain variable and the closed-loop TF analysis. As a result, the carrier synchronization scheme is constructed by an *outer* and an *inner* loops, which can be viewed as a *proportional* and a *integral* parts of DPLL, respectively. The gain equalization scheme is a first-order closed-loop built on each subchannel.

## REFERENCES

- [1] C. F. Wu, M. T. Shiue and C. K. Wang, "Joint Carrier Synchronization and Equalization for OFDM Systems over Multipath Fading Channel," *IEEE 68th Vehicular Technology Conf.*, pp. 1-5, Sept. 2008.
- [2] C. F. Wu, M. T. Shiue and C. K. Wang, "Joint Carrier Synchronization and Equalization Algorithm for Packet-Based OFDM Systems Over The Multipath Fading Channel," *IEEE Trans. on Vehicular Technology*, vol. 59, no. 1, pp. 248-260, Jan. 2010.
- [3] M. Speth, S. A. Fechtel, G. Fock and H. Meyer, "Optimal Receiver Design for Broad-Band Systems Using OFDM--Part I," *IEEE Trans. on Comm.*, vol. 47, no. 11, pp. 1668-1677, Nov. 1999.
- [4] K. Shi, E. Serpedin and P. Ciblat, "Decision-Directed Fine Synchronization in OFDM Systems," *IEEE Trans. on Comm.*, vol. 53, no. 3, pp. 408-412, Mar. 2005.
- [5] Floyd M. Gardner, *Phaselock Techniques*, Wiley, 3rd ed., 2005.
- [6] A. A. M. Saleh, R. A. Valenzuela, "A Statistical Model for Indoor Multipath Propagation," *IEEE J. on Selected Areas in Comm.*, vol. SAC-5, no. 2, pp. 128-137, Feb. 1987.

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