

Temperature Effect on the I-V Characteristics of the MOSFET Transistor

Ouassila Benzaoui^{1,2} and Cherifa Azizi³

1. Technology Department, Faculty of Technology, 20 August 1955 University, BP 26, Skikda 21000, Algeria.

2. Department of Physics, Faculty of Science, Mentouri Brothers University, Constantine 25000, Algeria

Email: o.benzaoui@gmail.com

3. Sciences Institute, Faculty of exact sciences, Larbi Ben M'hidi University, BP 358, Constantine Street, Oum El Bouaghi 04000, Algeria

Email: azizichhe@gmail.com

Abstract-- MOSFET Transistor occupies a fundamental place among all the components produced in micro-electronics. It was the subject of many studies and research to exploit its interesting and promising characteristics.

Owing to the fact that the semiconductors are very sensitive to the temperature, it is paramount to understand the phenomena that it involves. The aim of this contribution is the study of the temperature effect on the static I-V characteristics of the MOSFET.

The study enables us to calculate the drain current as a function of bias in both linear and saturated modes using a numerical simulation program; one could notice that the MOS transistor characteristics are very sensitive to the temperature. The inversion charge via the threshold voltage and the charge carrier mobility are the two principal influenced parameters. It was noted that the increase in the temperature induces a drop of the threshold voltage and carrier mobility. An immediate consequence of this reduction is the decrease in the drain current.

One can thus conclude that the temperature influences the performances of the device; the lower the temperature, the better is the reliability of the device under operation.

Index Term-- MOSFET; Temperature; Mobility; Performances.

I. INTRODUCTION

The MOS transistor is by far, the device the most encountered in the current production of semiconductor components, several acronyms are used in the literature to describe the MOS transistor (Metal Oxide Semiconductor): MOSFET (MOS Field Effect Transistor), IGFET (Insulated Gate Field Effect Transistor) and MOST (Metal Oxide Semiconductor Transistor) [1].

Silicon technologies field-effect MOSFET transistors are very mature and offer components with very honorable performances because of the intrinsic physical properties at relatively low cost. This remains a major asset in the current context making it possible to fulfill the requirements of communication systems in terms of power.

The transistors are traditionally modulated by using the model of the equivalent diagram. However, this kind of models can only give one limited outline on the physical behavior of the component, which is why the physical models based on analytical description intervene, in terms of transport properties, geometrical and technological parameters of the transistor.

II. CALCULATION OF THE DRAIN CURRENT

The figure (1) represents the elementary structure of the studied device; it is a N type MOSFET working in the static regime, its modeling requires several simplifications due to the difficulties imposed by the avalanche phenomena (substrate-drain junction) and source-drain drilling [2].

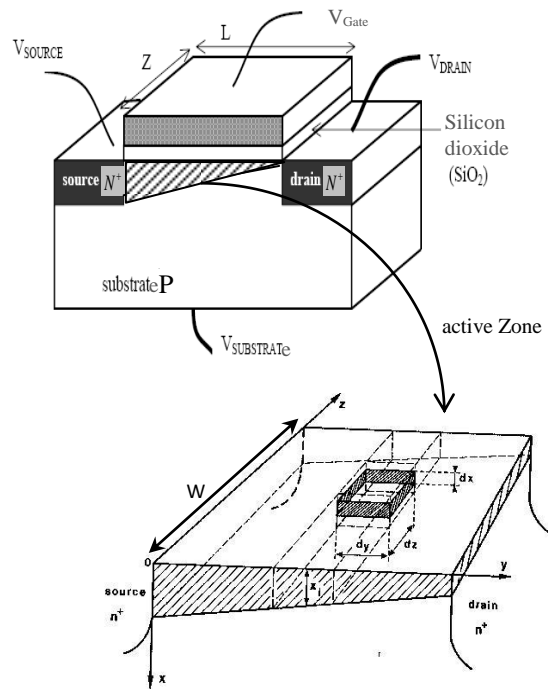


Fig. 1. Structure of the MOSFET type N

To calculate the drain current of the MOSFET one adopts the following assumptions [3]:

- The insulator (SiO_2) is ideal: absence of charge traps in insulator and at the interface of the semiconductor. There is no difference in work between metal and the semiconductor.
- The mobility of the carriers is constant in the inversion layer.
- The doping of the channel is uniform in all the substrate.
- The leakage current is negligible.

- Approximation of the gradual charge: The transverse field E_x in the channel is more important than the longitudinal field E_y .

Thus the variation of the drain current I_D with the drain-source voltage V_D and the gate-source voltage V_G is given by the following general relation [4]:

$$I_D = \frac{Z\mu C_{ox}}{L} \left(\left(V_G - \frac{V_D}{2} - 2\phi_{Fi} \right) V_D - \frac{2}{3} \frac{(2eN_a \epsilon_s)^{1/2}}{C_{ox}} \left((V_D + 2\phi_{Fi})^{3/2} - (2\phi_{Fi})^{3/2} \right) \right) \quad (1)$$

However, this equation is rewritten differently, according to the operation regime of the transistor which depends primarily on the value of the drain voltage V_D . These regimes are:

I. Linear regime

The drain voltage in this regime obeys to the following condition: $V_D \leq V_G - V_T$. Thus, the equation of drain current is rewritten [5]:

$$I_D = \frac{Z\mu C_{ox}}{L} (V_G - V_T) V_D \quad (2)$$

With V_T is the threshold voltage and C_{ox} is the insulator capacitance, both are given by:

$$V_T = 2\phi_{Fi} + (4eN_a \epsilon_s \phi_{Fi})^{1/2} / C_{ox} \quad (3)$$

$$C_{ox} = \frac{\epsilon_{ox}}{d} \quad (4)$$

II. Saturation regime

The drain voltage is conditioned by: $V_D > V_G - V_T$. The drain current becomes [5]:

$$I_{Dsat} = \frac{Z\mu C_{ox}}{2L} (V_G - V_T)^2 = \frac{Z\mu C_{ox}}{2L} V_{Dsat}^2 \quad (5)$$

Where V_{Dsat} is the saturation voltage given by:

$$V_{Dsat} = V_G - 2\phi_{Fi} = V_G - V_T \quad (6)$$

III. RESULTS AND DISCUSSIONS

For the numerical calculation of the drain current versus bias voltage, one uses the data of transistors MOSFET1 ($L=2.5\mu m$); MOSFET2 ($L=1.5\mu m$) whose parameters are given in table 1.

Table I

MOSFET	L (μm)	D (A°)	Z (cm)	N_a (cm^{-3})	μ_0 ($cm^2 \cdot s^{-1} \cdot v^{-1}$)	Φ_{Fi} (V)
MOSFET1	1.5	1500	3.53	10^{16}	277	0.35
MOSFET2	2.5	1000	2.81	10^{16}	360	0.35

The figures (2) and (3) represent the variation of the drain current I_D versus V_D for various values of V_G obtained

respectively for the MOSFET1 ($L=1.5\mu m$) and the MOSFET2 ($L=2.5\mu m$), one notes that the drain current I_D increases with the voltage V_D , then it saturates in the case of the MOSFET2 for a value for which the Space Charge Region (S.C.R) covers all the channel, contrary to the MOSFET1 which is saturated before the channel pinch. This is due to the fact that the length of the channel is short, which leads quickly to appreciable electric field values and consequently, fast saturation of the carriers velocity in the channel.

This means that the saturation of the drain current, in this case, is related to the saturation of the carriers velocity. It should be also noted that I_D undergoes a reduction until its annulment for a nonzero value of V_G known as threshold voltage.

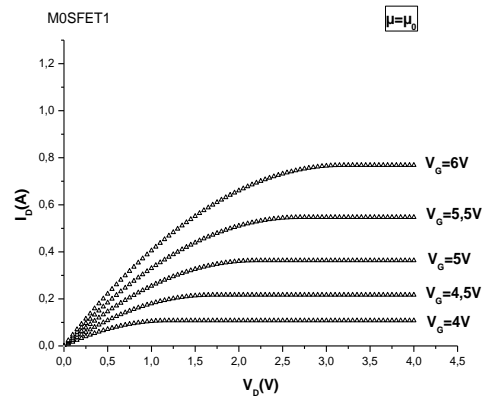


Fig. 2. Variation of I_D versus V_D for various V_G values for MOSFET1 transistor.

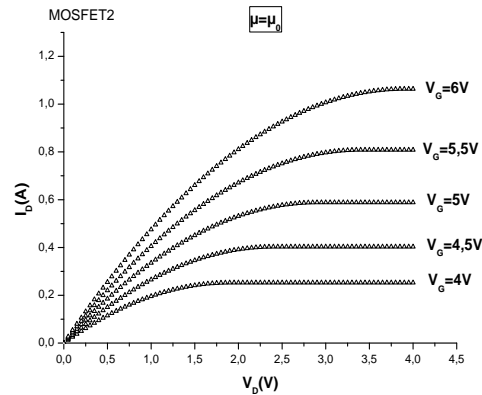


Fig. 3. Variation of I_D versus V_D for various V_G values for MOSFET2 transistor.

The mobility is a physical quantity defined as the proportionality factor between carriers velocity and the electric field, it depends in a complex way, on the nature and the frequency of the collisions and interactions undergone by the carriers during their displacement, it has a great influence on the current-voltage characteristics [5].

To show this dependence the two following laws were chosen:

$$\mu_1 = \frac{\mu_0}{1 + \theta(V_G - V_T) + E/E_c} \quad (7) \quad [4];$$

$$\mu_2 = \frac{\mu_0}{[1 + \theta(V_G - V_T)] \left[1 + E/E_c \right]} \quad (8) \quad [1]$$

μ_0 the electron mobility under low field, θ and E_c (critical field) are two parameters measured experimentally ($\theta[V^{-1}] = 1.5/d$, E_c is about $5 \cdot 10^4$ v/cm).

In fact, the use of these expressions for MOSFET1 transistor, enables us to obtain the figures (4) and (5) on which one notes that the variations of the drain current are maximum in the case of μ_1 . The current undergoes a reduction in the saturation regime which is remarkable in the case of the mobility μ_2 . This decrease is due to the fact that the accumulation phenomenon of the charge carriers occurring in the channel is not taken into account.

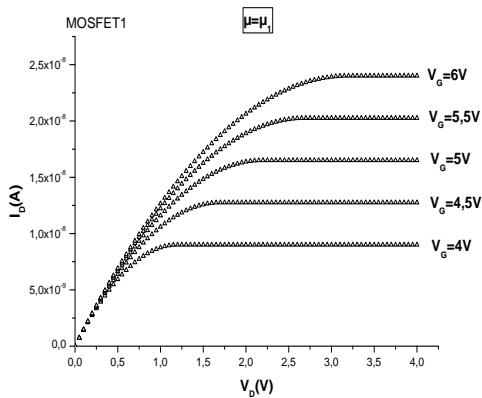


Fig. 4. Variation of I_D versus V_D for various V_G values obtained by using the expression of the mobility μ_1 .

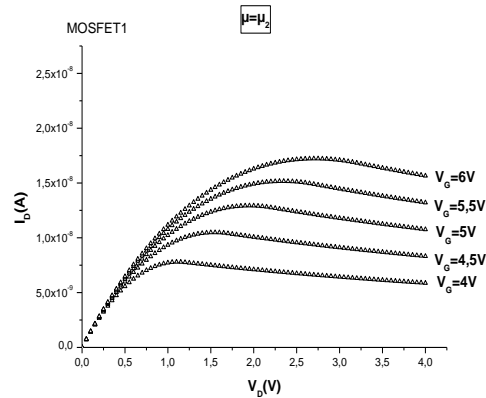


Fig. 5. Variation of I_D versus V_D for various V_G values obtained by using the expression of the mobility μ_2 .

V. EFFECT OF THE TEMPERATURE

The current characteristics of the MOSFET are strongly related to the temperature. However the majority of simulations suppose that the temperature of the component is constant. The room temperature (300 K) is usually taken as the component temperature.

The dependence of the carriers mobility on the temperature plays a fundamental role in the determination of the current. A simple law to model the variation of mobility with the temperature is the following one [6, 7, 8]:

$$\mu(T) = \mu(T_0) \left[\frac{T}{T_0} \right]^{-k} \quad (9)$$

The variation the saturation speed with the temperature for the MOSFET is given by [9]:

$$V_{sat} = \frac{2.4 \cdot 10^5}{1 + 0.8 \exp \left[\frac{T}{600} \right]} \quad (10)$$

The threshold voltage as a function of the temperature is given by [10, 11, 12]:

$$V_T(T) = V_T(T_0) [1 - \gamma(T - T_0)] \quad (11)$$

Where T is the temperature of the network, T_0 the room temperature (300k), K a factor varying between 2.2 and 2.7 and γ is an empirical coefficient in the range from 2 to 3 mV/k.

We studied the effect of the temperature on the static characteristics of the component, by numerical simulation using the mobility laws, the saturation speed and the threshold voltage. Calculation was carried out for MOSFET1 transistor.

The figure (5) presents the variation of the drain current I_D versus V_D for various temperatures. It can be seen that the drain current decreases with the temperature increase. This is an immediate consequence of the reduction of the mobility and the saturation speed as illustrated in figures (6) and (7) respectively.

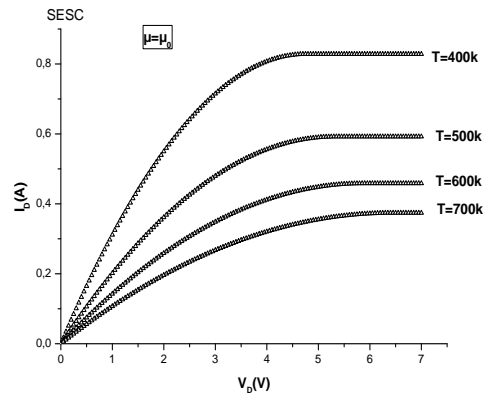


Fig. 5. Variation of I_D versus V_D for various temperature values.

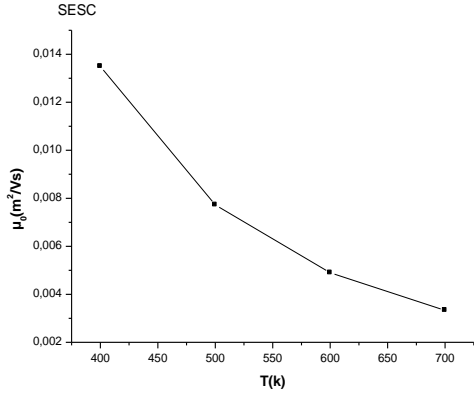


Fig. 6. Variation of mobility μ_0 versus temperature.

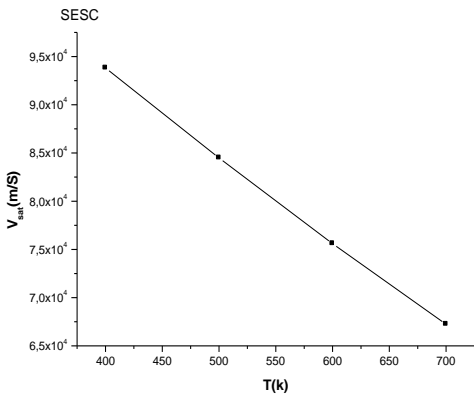


Fig. 7. Variation of saturation speed V_{Sat} versus the temperature.

It should be noted that the rise in the temperature induces an intensive interaction between charge carriers and the optical phonons of the network. This leads to the decrease of the mobility and a limitation of the saturation speed of the carriers for a critical value of the lateral field E_C . The latter constantly increases with the temperature (fig.8).

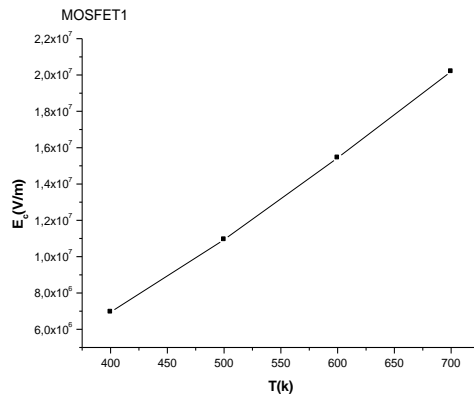


Fig. 8. Variation of the saturation of the electric field E_c versus the temperature.

The figures (9) and (10) show I-V characteristics in the case of variable mobilities μ_1 and μ_2 . The same explanation as in the case of constant mobility μ_0 can be given, i.e. the drain current is better at low temperature.

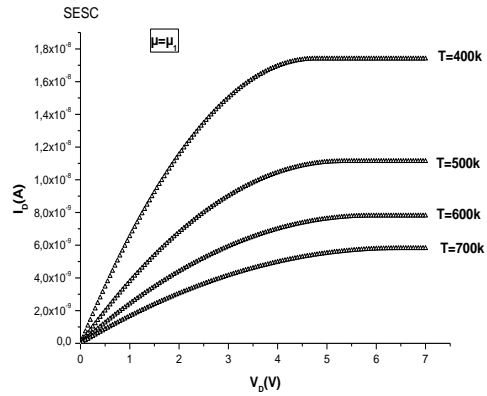


Fig. 9. Variation of I_D versus V_D for various temperatures values obtained by using the expression of the mobility μ_1 .

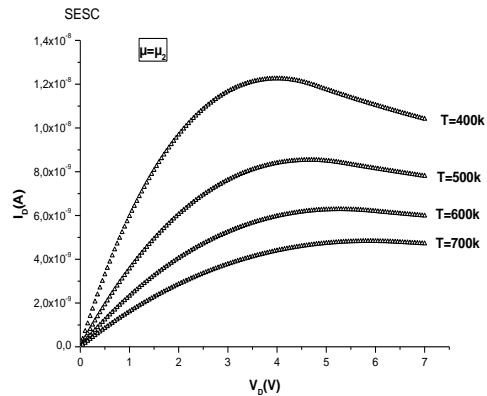


Fig. 10. Variation of I_D versus V_D for various temperatures values obtained by using the expression of the mobility μ_2 .

The variation of μ_1 and μ_2 mobilities versus the temperature are presented on the figure (11), they decrease as the temperature increases.

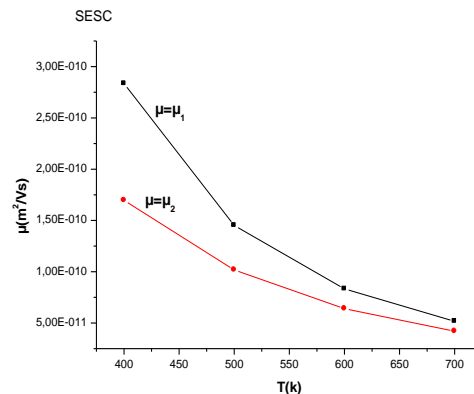


Fig. 11. Variation of μ_1 and μ_2 mobilities versus temperature.

VI. CONCLUSION

In this paper, we developed a model allowing the description of the static electric operation of MOSFET in linear and saturated regimes, by taking into account the variation of mobility versus the electric field. The mobility law in the MOSFET which gives maximum variations of the drain current is given by the expression (7).

In addition the variation of the I-V characteristics of the component versus the temperature were obtained; the lower the temperature, the better is the reliability of the device under operation.

REFERENCES

- [1] Skotnicki, T. : Transistor MOS et sa technologie de fabrication, Technique de l'ingénieur, traité Electronique, 1987.
- [2] Muller, D. : Optimisation des potentialités d'un transistor LDMOS pour l'intégration d'amplificateur de puissance RF sur Silicium, Thèse de Doctorat, Université Limoge, 61-2006.
- [3] SZE, S.M.: Physics of Semiconductor Devices, (2nd Edition). Taipei: John Wiley & sons, 1981.
- [4] Mathieu, H. : Physique des semi-conducteurs et des composants électroniques, (2nd Edition). Dunod, Paris, 2001.
- [5] Morancho, F. : Le transistor MOS de puissance à tranchées : Modélisation et Limites de Performance, Université Paul Sabatier, Toulouse, 1996, 96482.
- [6] Arora, N.D., Hauser, J.R., Roulston, D.J.: Electron and Hole Mobilities in Silicon as a function of Concentration and Temperature, IEEE Transaction On Electron Devices, Vol. 30, N°6, p. 658-663, 1983.
- [7] Klaassen, D.B.M.: A United Mobility Model for Device Simulation: II. Temperature Dependence of Carrier Mobility and Lifetime, Solid-State Electronics, Vol. 35, p. 961-967, 1992.
- [8] Dorkel, J.M., Leturq, P.: Carrier Mobilities in Silicon Semi-Empirically Related to Temperature, Doping and Injection Level, Solid-State Electronics, Vol. 24, p. 821-824, 1981.
- [9] Jacobini, C., Canali, C., Ottaviani, G., Alberigi Quaranta, A.: A Review of some Charge Transport Properties of Silicon, Solid-State Electronics, Vol. 20, p. 77-89, 1977.
- [10] Arora, N.D.: MOSFET Models for VLSI Circuit Simulation-Theory and Practice, Editions Springer Verlag, 1993.
- [11] Fatemizadeh, B., Silber, D.: Modeling of LDMOST and LIGBT Structures at High Temperatures, Proc. ISPSD and IC's, Suisse, 1994.
- [12] Pavlovic, Z., Prijic, Z., Dimitrijiev, S., Stojadinovic, N.: Temperature Dependence of On-Resistance in Low-Voltage Power VDMOS Transistors, Microelectronics Journal, Vol. 24, p. 115-124, 1993.